CLAIM:

1. A coprocessor (30) to a main processor (20) having an execution speed greater than that of said processor, the coprocessor comprising a two-dimensional array (108) of processing cells (112) and being communicatively connected to said processor by an interface module (40) having a mechanism (122, 124) for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

2. The coprocessor of claim 1, wherein the array comprises a systolic processing array (106).

3. The coprocessor of claim 1, wherein the paths are connected one-to-one with said respective cells (122, 124).

4. The coprocessor of claim 1, wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths (114).

5. The coprocessor of claim 1, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (108).

6. A coprocessing system including the coprocessor (30), interface module (40) and main processor (20) of

connects with the interface module and the main processor to provide the main processor to coprocessor connection.

7. The coprocessor of claim 1, including an array processor (106) that comprises said two-dimensional array.

8. An integrated circuit (102) comprising the coprocessor of claim 1.

9. A receiver (100) comprising the integrated circuit of claim 8.

10. The coprocessor of claim 1, wherein said array (108) is rectangular and said periphery consists of those of said processing cells located in at least one of a first row, last row, first column and last column of said array (112).

11. The coprocessor of claim 1, wherein said processor (20) comprises a digital signal processor.

12. The coprocessor of claim 1, wherein said processor (20) comprises a general purpose processor.

13. A functional unit (322) having a two-dimensional array (108) of processing cells (112) and serving as a component of a main processor (302), the unit having a mechanism (110) for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array (122, 124).

14. The unit of claim 13, wherein said processor comprises a very long instruction word (VLIW) processor (302).

15. The unit of claim 13, wherein inter-cell connection within the array (108) is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (112).

16. The unit of claim 13, further including means for transmitting (126, 128, 310, 412) a plurality of array programs to corresponding predetermined subsets of said processing cells (115).

17. A system including the processor of claim 16, and an array program generator (310) for generating the array programs to be transmitted, and, when needed, updating a program (406), transmitting the updated program (412), and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths (414, 416).

18. The system of claim 17, further including a compiler (312) configured for receiving, in response to said program updating (406, 408), data representative of input and output timing for said unit (410) and further

configured for compiling an instruction based on said data (310, 312).

19. An integrated circuit (306) comprising the processor of claim 13.

20. A method for interfacing a coprocessor (30) to a main processor (20), comprising the steps of:

configuring the coprocessor to comprise a two-dimensional array (108) of processing cells (112) and to have an execution speed greater than that of said processor; and

communicatively connecting the coprocessor to said processor by an interface module (40) having a mechanism (110) for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array (122, 124).